



## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: HOSHI, Kenji et al.

Group Art Unit: 2814

Serial No.: 10/073,314

Examiner: TRINH, HOA B.

Filed: February 13, 2002

P.T.O. Confirmation No.: 4466

For:

SEMICONDUCTOR DEVICE AND ALIGNMENT SENSING

METHOD FOR SEMICONDUCTOR DEVICE

## **AMENDMENT UNDER 37 CFR §1.111**

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

May 30, 2003

Sir:

In response to the Office Action dated March 5, 2003, please amend the above-identified application as follows:

## **IN THE CLAIMS:**

1. (Amended) A semiconductor device comprising a plurality of alignment marks formed over a semiconductor wafer,

each of the alignment marks being divided by a micronized pattern,

the micronized pattern having a size smaller than a resolution limit of an alignment sensor,

<u>and</u>

the micronized pattern having a pattern forming margin larger than that of a device pattern formed over the semiconductor wafer has.